**In the Claims:**

1-14. (Canceled)

15. (Original) A method of forming a semiconductor chip carrier, comprising the steps of:

providing a substrate, having a plated through hole therein;

depositing a redistribution layer on a first and a second surface of the substrate; and

forming a via within the redistribution layer, selectively positioned over and electrically contacting the plated through hole.

16. (Original) The method of claim 15, further including the step of:

forming a chip connection pad in the via.

17. (Original) The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein includes the steps of:

drilling a hole through the substrate;

cleaning the hole; and

forming a conductive layer on an interior surface of the hole.

18. (Original) The method of claim 15, further comprising the step of:

filling the plated through hole with a reinforcing material.

19. (Original) The method of claim 18, wherein the reinforcing material comprises an electrically conductive material.

20. (Original) The method of claim 15, wherein the step of depositing the redistribution layer is performed using a lamination process.

21. (Original) The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein further includes the steps of:

providing a ground plane;

forming a first pair of signal planes within the substrate;

forming a first pair of power cores within the substrate;

forming a second pair of signal planes within the substrate; and

forming a second pair of power cores within the substrate.

22. (Original) The method of claim 21, wherein the first and second pair of signal planes are controlled impedance circuitry.

23. (Original) The method of claim 21, wherein the second pair of power cores are directly underneath and electrically connected to portions of the redistribution layer.

24. (Original) The method of claim 23, wherein the second pair of power cores further includes a top surface metallurgy (TSM) and a bottom surface metallurgy (BSM).

25. (Original) The method of claim 15, wherein the redistribution layer comprises a fatigue resistant dielectric material.

26. (Original) The method of claim 15, further comprising the step of:

providing a buried plated through hole in the substrate.

27-29. (Canceled)